Claim 1, 40 and 42 were rejected under 35 U.S.C. § 102(b) as being anticipated by Asano et al. (U.S. Patent No. 4,612,462, "Asano"). However, Applicants respectfully submit that claim 1 recites subject matter that is neither disclosed nor suggested in Asano.

Applicants amended claim 1 recites a level shift circuit that includes a capacitor and a charge control circuit connected to the capacitor for providing a voltage of a high potential power supply to the capacitor and controlling charging of the capacitor. A limiting circuit is connected to the high potential power supply and the charge control circuit for limiting the voltage provided to the capacitor from the high potential power supply, before the charge control circuit stops providing the voltage of the high potential power supply to the capacitor. The limiting circuit limits the voltage provided to the capacitor when the boosting of an output signal of the level shift circuit to a boosted voltage, which is higher than the voltage of the high potential power supply, is started.

In making this rejection, the Office Action took the position that Asano discloses all of the elements of the claimed invention. However, it is respectfully submitted that the prior art fails to disclose or suggest the structure of the claimed invention, and therefore, fails to provide the advantages of the present invention. For example, the shift level circuit of the present invention includes a capacitor and a charge control circuit connected to the capacitor that provides a voltage of a high potential power supply to the capacitor and also controls the capacitor. A limiting circuit is connected to the high potential power supply and the charge control circuit for limiting the voltage provided to the capacitor from the high potential power supply, before the charge control circuit stops providing the voltage of the high potential power supply to the capacitor.

As a result of this claimed configuration, when the capacitor performs voltage step-up, the current limiting circuit limits the charge that leaks from the capacitor to the high potential power supply and increases the voltage step-up efficiency. This improves the response of the output signal in the level shift circuit.

The present invention is directed to a level shift circuit that includes a limiting circuit connected to a high potential power supply and a charge control circuit. The limiting circuit limits the voltage provided to a capacitor from the high potential power supply before the charge control circuit stops providing the voltage of the high potential power supply to the capacitor. That is, the limiting circuit limits the voltage provided to the capacitor when the boosting of an output signal of the level shift circuit to a boosted voltage, which is higher than the voltage of the high potential power supply, is started.

Asano discloses a logic circuit that includes a voltage booster (15). The voltage booster (15) includes a capacitor (14), MOS transistors (81, 83), and an inverter (13). When an input signal goes to logical level "1," the MOS transistors (81, 83) turn on at the same time in response to an output signal of the inverter (13) and steadily provide a boosted voltage (VH) from a boosted voltage retention circuit (70) to a signal output end B (capacitor (14)).

The Office Action asserted that the MOS transistor (81) of Asano corresponds to the limiting circuit of the present invention and the MOS transistor (83) of Asano corresponds to the charge control circuit of the present invention. However, Asano does not disclose limiting the voltage provided to the capacitor. Asano discloses the MOS transistor (81) that steadily provides the boosted voltage (VH) to the capacitor (14) when the voltage booster (15) performs voltage boosting. (See col. 5, lines 19-31).

This is contrary to the present invention where the limiting circuit limits the voltage provided to the capacitor when the boosting of an output signal of the level shift circuit to a boosted voltage, which is higher than the voltage of the high potential power supply, is started, as recited in amended claim 1.

As claims 40-42 depend directly or indirectly from claim 1, Applicants respectfully submit that each of these claims incorporate the patentable aspects thereof, and are therefore allowable for at least same reasons as discussed above.

Therefore, it is respectfully submitted that the Applicants' invention, as set forth in claim 1, is not anticipated within the meaning of 35 U.S.C. § 102.

Claims 1 and 36-42 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Schmitt et al. (U.S. Patent No. 6,130,556, "Schmitt") in view of Kushiyama (U.S. Patent No. 5,933,028). In making this rejection, the Office Action took the position that Schmitt discloses all the elements of the claimed invention, with the exception of a capacitor coupled to anode AN. Kushiyama is cited for disclosing this limitation.

Applicants amended claim 36 includes a level shift circuit that includes a capacitor. A first transistor is connected to the capacitor for providing a voltage of a high potential power supply to the capacitor and controlling charging of the capacitor. A second transistor is connected to the high potential power supply and the first transistor for being turned off before the first transistor is turned off when the boosting of an output signal of the level shift circuit to a boosted voltage, which is higher than the voltage of the high potential power supply, is started.

As will be discussed below, applicants respectfully submit that claims 1-6 recite subject matter that is neither disclosed nor suggested by any combination of the prior art.

Fig. 3A of Schmitt discloses a pull-down control circuit (16) that includes a first transistor (MP1) and a second transistor (MP2).

Kushiyama discloses a driving circuit that includes a capacitor (15) coupled to the output of level shifter circuit (11, 12, 13) as shown in Fig. 1 of Kushiyama.

However, neither Schmitt nor Kushiyama discloses that the limiting circuit limits the voltage provided to the capacitor when the boosting of an output signal of the level shift circuit to a boosted voltage, which is higher than the voltage of the high potential power supply, is started, as recited in amended claim 1. Furthermore, neither Schmitt nor Kushiyama discloses a second transistor connected to the high potential power supply and the first transistor for being turned off before the first transistor is turned off when the boosting of an output signal of the level shift circuit to a boosted voltage, which is higher than the voltage of the high potential power supply, is started, as recited in amended claim 36.

Still further, because claims 40-42 are directly or indirectly dependent on claim 1 and claims 37-39 are dependent on claim 36, Applicants submit that these claims recite subject matter that is neither disclosed nor suggested by the cited prior art, for at least the reasons set forth above with respect to the independent claims.

Therefore, as discussed above, Applicants submit that Schmitt and Kushiyama either alone or in combination, fail to disclose or suggest the claimed invention.

Thus, it is respectfully submitted that the Applicants' invention, as set forth in claim 3, is not obvious in view of any combination of the prior art within the meaning of 35 U.S.C. § 103.

New added claim 43 further recites that the limiting circuit limits the voltage provided to the capacitor when the charging of the capacitor to a boosted voltage, which is higher than the voltage of the high potential power supply, is started.

Newly added claim 44 further recites that the second transistor is turned off simultaneously when the charging of the capacitor to the boosted voltage is started.

Newly added claim 45 further recites that the limiting circuit is connected to the high potential power supply and the charge control circuit, for limiting the voltage provided to the capacitor from the high potential power supply simultaneously when the boosting of an output signal of the level shift circuit to a boosted voltage, which is higher than the voltage of the high potential power supply, is started.

Newly added claim 46 further recites that the limiting circuit is connected to the high potential power supply and the charge control circuit, for limiting the voltage provided to the capacitor from the high potential power supply simultaneously when the charging of the capacitor to a boosted voltage, which is higher than the voltage of the high potential power supply, is started

Therefore, it is respectfully submitted that the newly-added claims are also patentable over the applied references.

In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of claims 1 and 36-46, claims 2-10 already being allowed, and the prompt issuance of a Notice of Allowability are respectfully solicited.

Should the Examiner believe anything further is desirable in order to place this application in better condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

In the event this paper is not considered to be timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108075-00054.**

Respectfully submitted,
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Enclosures: Marked-Up Copy of Amended Claims
Request for Continued Examination
Petition for Extension of Time (two months)
Extra Claims Fee Transmittal

MARKED-UP COPY OF AMENDED CLAIMS

1. (Amended) A level shift circuit comprising:

a capacitor;

a charge control circuit connected to the capacitor for providing a voltage of a high potential power supply to the capacitor and controlling charging of the capacitor; and

a limiting circuit connected to the high potential power supply and the charge control circuit for limiting the voltage provided to the capacitor from the high potential power supply before the charge control circuit stops providing the voltage of the high potential power supply to the capacitor,

wherein the limiting circuit limits the voltage provided to the capacitor when the boosting of an output signal of the level shift circuit to a boosted voltage, which is higher than the voltage of the high potential power supply, is started.

36. (Amended) A level shift circuit comprising:

a capacitor;

a first transistor connected to the capacitor for providing a voltage of a high potential power supply to the capacitor and controlling charging of the capacitor; and

a second transistor connected to the high potential power supply and the first transistor for being turned off before the first transistor is turned off when the boosting of an output signal of the level shift circuit to a boosted voltage, which is higher than the voltage of the high potential power supply, is started.